CHAPTER 4:
MOST PROCESSING TECHNOLOGY
Introduction

Objectives:
1. Discuss the fundamentals of MOST chip fabrication and examined the major steps of the process flow
2. Emphasis only on the general outline of process flow and the interaction of various processing steps, which ultimately determine the device & circuit performance
3. To show that there are very strong links between the fabrication process, circuit design process and the performance of the resulting chip
4. Start with an introduction to semiconductor manufacturing process, then to NMOS processing flow and finally to CMOS fabrication steps
5. Later the Layout design rules will be cover
Silicon Semiconductor Manufacturing Technology

Overview

- Semiconductor? Silicon or Germanium
- Why called as semiconductor? Conductivity between conductor & insulator
- How to change this conductivity? Introducing impurity atoms or dopants
- 2 type of dopants? Electron or Holes
- Impurity use electron = acceptors else donors
- Si contains majority of donors = n-type else p-type
- When p & n-type brought together = junction = diode
- When make 2 junction = pnp or npn = bipolar
- When make metal-oxide-semiconductor = MOST
Wafer processing

- Wafer is a disk of Silicon varies from 75mm to 230mm and less than 1mm thick
- Wafer are cut from ingots of single-crystal silicon that been pulled from crucible melt of pure molten polycrystalline silicon
Oxidation

- Process to make SiO$_2$
- Achieved by heating Si wafers in an oxidizing atmosphere such as oxygen or water vapor

2 common approaches:
1. Wet Oxidation: When oxidizing atmosphere is water vapor with temperature between 900°C & 1000°C that rapidly process
2. Dry Oxidation: When oxidizing atmosphere is purely oxygen with temperature in range of 1200°C

- The oxidation process consumes silicon
Epitaxy, Deposition, Ion-Implantation & Diffusion, Etching

- Epitaxy - growing a thin single-crystal film on silicon surface by subjecting the surface to elevated temperature and a source of dopant material
- Deposition - Evaporating dopant material onto the silicon surface followed by a thermal cycle, which is used to drive the impurities from surface of silicon into the bulk
- Ion-Implantation - Subjecting the silicon substrate to highly energized donor or acceptor atom that makes the atom travel below the surface, forming regions with varying doping concentrations
- Diffusion - Occur at temperature > 800°C between any silicon that has differing densities of impurities, with impurities tend to diffuse from areas of high concentration to low
- Etching - Removing unwanted layers on silicon surfaces either using wet or dry etching depending on required pattern
Basic Steps of Fabrication Process Flow

- Construction of transistors depends on the ability to control where & how many & what type of impurities are introduced into silicon wafer

- What Material of impurities/dopant source:
  1. Boron – for acceptor silicon (p-type)
  2. Arsenic / Phosphorus – donor (n-type)

- How much? Determined by the energy (in eV) & time of ion-implantation or the time & temperature of deposition & diffusion steps

- Where it used determine by using special materials called as masks - In places covered by mask, the ion-implantation does not occur else it will occur

- 4 type of material commonly used for masking:
  1. Photoresist
  2. Polysilicon
  3. Silicon dioxide (SiO₂)
  4. Silicon nitride (SiN)

- Thus, we could say that the basic of fabrication process steps requires that certain area are defined on wafer / chip by appropriate masks that can be viewed as creating a different layer for different material
In general, a layer must be patterned before next layer of material is applied on chip.

"Photolithography" is the process used to transfer a pattern to a layer on the chip that must be repeated for each layer since it has its own distinct patterning requirement by using different masks.

Thus, masking process involve:

1. Patternning “windows’ in a mask material on the surface of wafer
2. Subjecting exposed areas to a dopant source
3. Removing any unwanted mask material
SiO₂ Patterning

1. Silicon Wafer

2. Create oxide layer on Si Surface

3. Deposition of photoresist layer on top of oxide, which is essentially light-sensitive, acid-resistant organic polymer & initially insoluble

4. If photoresist exposed to UV light, exposed areas becomes soluble so that the region are no longer resistant to etching solvents. It is done by selectively covered the opaque features on the glass mask.

- Positive photoresist - initially insoluble and becomes soluble when expose to UV
- Negative photoresist - initially soluble and becomes insoluble when expose to UV
Continued...

Chemical etch (HF acid) or dry etch (plasma)

5. Etched away oxide regions not covered by hardened photoresist using either Chemical etch (HF acid) or dry etch (plasma) process

6. End of etch process will obtain oxide window that reaches down to the silicon surfaces

7. Stripped out the remaining photoresist from oxide surface using another solvent, leaving the patterned oxide feature on the surface of silicon
Note:

- Previous sequence of process only for a single pattern transfer onto oxide surface, the fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon & metal.

- However, the basic of patterning process used in fabrication process is quite similar to discuss oxide patterning.

- For accurate generation of high density patterns required in sub-micron devices, electron beam (E-beam) lithography is used instead of optical lithography.
Fabrication of the MOS transistor

1. Silicon Wafer

2. Create oxide layer on Si Surface - Oxidation

3. SiO₂ patterning - Selectively etched oxide to expose Si surface on which MOST will be created

4. Deposit a thin, high-quality oxide layer on surface which will be the gate oxide of MOST

5. Deposit polySi that used for both as gate electrode & interconnect medium in Si Chip. PolySi has high resistivity & reduce by doping it with impurity atom

6. Patterned & etched polySi to form interconnects & MOST gates

7. Etched away thin & single oxide not cover by PolySi, which exposed bare Si Surface on which source & drain junctions are to be formed
8. Doped the entire si surface with high conc. Of impurities by an ion implantation (donor - n-type or acceptor -p-type). We see that doping impurities penetrates the exposed areas on si surface, ultimately creating 2 n-type regions for source & drain in the p-type substrate. Also it penetrates the polysi on surface & reduce it resistivity. Note that polysi gate that patterned before doping actually define the precise location of channel region and hence the source & drain regions. This called as ‘self-aligned process’ since it allows a very precise positioning of the 2 regions relative to gate.

9. Entire si surface is again covered by an insulating oxide and then patterned to provide a contact windows for drain & source junctions.

10. Entire si surface is covered with evaporated aluminium which will form the interconnects and finally patterned & etched completing the interconnection of the MOST on the surfaces.
Device Isolation Techniques

- MOST that comprises of IC must be electrically isolated from each other during fabrication
- Isolation important for:
  1. Preventing unwanted conduction paths between devices
  2. Avoiding creation of inversion layers outside channel region of transistors
  3. Reducing leakage currents
- How? The devices are typically created in dedicated regions called “active areas”, where each active areas is surrounded by a relatively thick oxide barrier called “field oxide”
- One method has been discussed previously, where a thick field oxide grows on the entire Si surface and then selectively etches oxides in certain regions, to define active areas.
- This method has some drawbacks:
  1. Thickness of field oxide will lead to rather large oxide steps at boundaries between active areas and isolation regions
  2. When polySi & metal layers are deposited over such boundaries in subsequent processes, the sheer height differences at the boundary can cause cracking of deposited layers, leading to chip failure.
- To prevent it, most manufacturers prefer a method that partially recesses the field oxide into Si surface, resulting in more planar surface topology called LOCOS - Local Oxidation of Silicon
LOCOS

- Technique based on selectively *growing* the field oxide in certain regions, instead of selectively *etching* away the active areas after oxide growth.

- Selectively oxide growth achieved by shielding active areas with Silicon Nitride (Si$_3$N$_4$) during oxidation, which effectively inhibits oxide growth.

1. Thin pad oxide grown on Si Surface, followed by deposition & patterning of Si$_3$N$_4$ to mask/define active area.

2. Thin pad oxide underneath Si$_3$N$_4$ used to protect Si Surface from stress caused by nitride during an ion implantation of p-type to create channel-stop implants that surround the transistors.

3. Thick oxide is grown in area not covered by Si$_3$N$_4$. Note that field oxide is partially recessed into surface since thermal oxidation also consumes Si. Also, the field oxide forms a lateral extension under nitride layer, called as ‘bird beak’ that responsibly for reduction of active area.

4. Finally, nitride & thin pad oxide etch away resulting in active areas surrounded by partially recessed field oxide.

Note:

1. LOCOS is a popular method for achieving field oxide isolation with more planar surface topology.

2. Several additional measures have also been developed over the years to control lateral ‘bird beak’ encroachment, since it will ultimately limit the device scaling & density in VLSI circuits.
Figure 2.5 Basic steps of the LOCOS process to create oxide isolation around active areas.
Multilevel Interconnects and Metallization

- Metal layers are needed for:
  1. Creating interconnections between transistors
  2. Routing power supply, signal & clock lines on chip surface
- Availability of multiple metal layers, where each are electrically isolated from neighboring layers by a dielectrics (SiO₂) allow:
  1. Higher integration densities for realization of complex design
  2. Adds third dimension that can be utilized very effectively in design
- The electrical connections between layers are made by ‘vias’ that placed wherever such contact needed, that each via formed by:
  1. Creating a window in isolation oxide before each new metallization step
  2. Filling the opening oxide with special metal plug, usually tungsten to make via
- Following vias, the new layer of metal deposition & patterning will forms the next metallization level.
- Noted that the chip surface is highly nonplanar due to previous process steps to create the transistors, such as n-well or p-well creation, local oxidation & gate formation.
- Also it is not desirable to deposit multiple metal interconnects lines directly on this uneven surface topography since:
  1. It may exhibit localized thinning & discontinuities at uneven surface edge
  2. Photolithography is also difficult & imprecise
  3. May eventually result in pronounced hills & valleys on the chip surface
- To avoid this problems of unplanar surface, the surface usually are planarized or flattened before each new metal deposition step by:
  1. A fairly thick SiO₂ layer is deposited on surface to cover all existing surface ununiformities.
  2. Then it planarized using several method such as glass reflow, etch-back or Chemical Mechanical Polishing (CMP) that used abrasive silica slurry is commonly adopted in industries.
Basic CMOS Technology

- Will discuss on n-well CMOS technologies, with a simplified treatment of process steps.
- This is necessary as it will be used as a guide for a better appreciation of the layout styles that used to implement CMOS gates.
- 4 main CMOS technologies:
  1. n-well process
  2. p-well process
  3. Twin-tub process
  4. Silicon on Insulator (SOI)
- During discussion of CMOS technologies, process cross sections and layouts will be presented. Fig. 3.6 summarizes the drawing conventions
Figure 3.6 CMOS process and layout drawing conventions
A Basic n-well Process

1. Creation of n-well: (fig. 3.7a)
   - Moderately doped (impurity conc. Less than $10^{15}$ cm$^{-3}$) p-type Si substrate
   - Initial oxide layer grown on entire surface
   - First lithographic mask (n-well mask) defines n-well region by an implanted of donor atoms, usually phosphorus into this window in oxide

2. Definition of Active areas & Field oxide (FOX) growth:
   - Using LOCOS technique with p-type (Boron) implanted & n-well channel stop (resist) mask, fig 3.7b & c
   - Stripped photoresist mask, leave the previously masked SiO$_2$/SiN sandwich defining active areas, fig 3.7d
   - Follow by growth thick Field Oxide (FOX) where SiN is absent, fig 3.7d

3. Polysilicon Deposition: (fig. 3.7e)
   - Involves deposition of polySi into surface & then etching the required pattern (inverted “U”) after completed previous steps of LOCOS

4. Source/Drain region Implantation:
   - By using n+ mask, the thin-oxide & polySi areas implanted by n-type ion that will create a self-align n+ diffusion areas underneath thin-oxide surface to be an nmos transistor source & drain region, fig. 3.7f
   - In modern small dimension processes, to reduce hot-carrier effects, the LDD (Lightly Doped Drain) method was used as shown in fig. 3.7g
   - By using p+ mask, the other thin-oxide & polySi areas implanted by p-type ion that will create a self-align p+ diffusion areas underneath thin-oxide surface into n-well region to be finally as an pmos transistor source & drain region, fig. 3.7h
5. Oxide (SiO$_2$) Deposition and contact Hole Etch:
- Deposit the entire surface with SiO$_2$ and then etch or patterning it down to the surface to be a contact hole, fig. 3.7i
- These will allows metal (next step) to contact with diffusion or polySi regions

6. Interconnection & Metallization:
- Metallization is then applied to the surface and selectively etched (fig. 3.7j) to produce circuit interconnections.
FIGURE 3.7 A typical n-well CMOS process
FIGURE 3.8 Cross section of a CMOS inverter in an n-well process
Cross-section

- Fig. 3.8c shows the cross-section of the finished n-well process.
- The layout of the n-well CMOS transistor corresponding to this cross-section is illustrated in fig. 3.8b.
- The corresponding schematic (for inverter) is shown in fig. 3.8a.
- From this fig. 3.8, it is evident that p-type substrate accommodates n-channel devices, whereas the n-well accommodates p-channel devices.
- Fig. 3.8 also appear in color as in plate 1.
1. MESH Definition

go athena
# mesh definition
line x loc=0.00 spac=0.100
line x loc=0.20 spac=0.006
line x loc=0.40 spac=0.006
line x loc=0.60 spac=0.010
#
line y loc=0.00 spac=0.002
line y loc=0.20 spac=0.005
line y loc=0.50 spac=0.050
line y loc=0.80 spac=0.150
2. Initial Substrate

- Phosphorus Impurity to form a n-type substrate on Silicon

# Initial Substate.
init silicon c.phosphor=1.0e14 orientation=100 two.d struct outfile=NMOS021.str
3. Forming p-type substrate

- Implant Boron to form a p-type substrate

```plaintext
# Implantasi Boron untuk menjadikan substrat jenis-P
implant boron dose=8.0e12 energy=100 tilt=0
rotation=0 crystal lat.ratio1=1.0 \nlat.ratio2=1.0
struct outfile=NMOS022.str
```
4. Diffusion to enhance p-type substrate quality

# Resapan berulang-ulang lapisan oksida yang bertujuan untuk memulihkan substrat-P.
diffus time=10 temp=950 weto2 press=1.00 hcl.pc=3
# Resapan dilakukan
diffus time=62 temp=950 t.final=1200 dryo2 press=1.00 hcl.pc=3
# Resapan dilakukan
diffus time=220 temp=1200 nitro press=1.00
# Resapan dilakukan
diffus time=90 temp=1200 t.final=800 nitro press=1.00
struct outfile=NMOS023.str
5. Etching all the SiO$_2$

# Pembersihan lapisan oksida pada permukaan substrat.
etch oxide all
struct outfile=NMOS024.str
6. Growth of Oxide layer by an oxidation process

# Lapisan oksida ditumbuhkan dengan teknik resapan basah.
diffus time=11 temp=950 dryo2 press=1.00 hcl.pc=3
struct outfile=NMOS025.str
7. Implantation of Boron p-type to adjust the threshold voltage

# Penyelarasan voltan ambang dengan membuat implantasi boron.
implant boron dose=9.5e11 energy=10 tilt=0 rotation=0 amorph lat.ratio1=1.0 \ lat.ratio2=1.0
struct outfile=NMOS026.str
8. Deposit Polysilicon as a gate electrode and etching

# Penumbuhan get polisilikon dengan menggunakan teknik endapan.
deposit poly thick=0.20 divisions=10
# Selepas ditumbuhkan get ini dipunarkan.
etch poly left p1.x=0.40
struct outfile=NMOS027.str
9. Oxidation process to enhance gate quality

# Pembentukan lapisan oksida pada get polisilikon dan subtrat untuk menghilangkan ke cacatan.

method compress init.time=0.10 fermi
diffus time=3 temp=900 weto2 press=1.00
hcl_pc=3
struct outfile=NMOS028.str
10. Implantation of phosphorus n-type of forming n+ region

# Pengedopan get polisilikon yang menyebabkan saluran-n dan telaga n+ terbentuk pada substrat.

implant phosphor dose=4.0e14 energy=20 tilt=0 rotation=0 amorph \ lat.ratio1=1.0 lat.ratio2=1.0 struct outfile=NMOS029.str
11. Deposit thick oxide

# Pembentukan ruangan oksida pada bahagian tepi get polisilikon.
deposit oxide thick=0.12 divisions=8
struct outfile=NMOS030.str
12. Etching oxide to form good isolation

# Lapisan ruangan oksida di atas substrat dibersihkan

etch oxide dry thick=0.12
struct outfile=NMOS031.str
13. Implantation of arsenic n-type for forming both source and drain region

# Pembentukan kawasan sumber dan salir.
implant arsenic dose=4.9e11 energy=50 tilt=0 rotation=0 amorph lat.ratio1=1.0 \ lat.ratio2=1.0
struct outfile=NMOS032.str
14. Oxidation to enhance S/D region

# Pemulihan kawasan sumber/salir
method compress init.time=0.10 fermi
diffus time=1 temp=900 nitro press=1.00
struct outfile=NMOS033.str
15. Etching oxide to form S/D window
# Pembukaan tingkap kawasan salir dan sumber pada bahagian atas substrat.
etch oxide left p1.x=0.20
struct outfile=NMOS034.str
16. Deposit Aluminum as the contact
# Pembentukan lapisan aluminium menggunakan kaedah endapan.
deposit alumin thick=0.03 divisions=2
struct outfile=NMOS035.str
17. Etching Al as the S/D contact

# Pembentukan terminal get, sumber dan salir.
etch aluminum right p1.x=0.10
20. Mirror the structure to have a complete nmos transistor

#Struktur dicerminkan untuk mendapat peranti nMOS penuh
struct mirror right
struc outfile=NMOS040.str
21. Naming all the electrode or contact

#Penamaan terminal nMOS.
electrode name=gate x=0.50 y=0.10
#
electrode name=source x=0.10
#
electrode name=drain x=1.10
#
electrode name=substrate backside
struc outfile=NMOS043.str
structure outfile=finaldevice-a.str
quit
Characterization: ATLAS

1. Specified structure device

go atlas
#
mesh infile=finaldevice-a.str
tonyplot finaldevice-a.str
#
2. Models : For Numerical Computation

#
models cvt srh boltzman print temperature=300
#
 mobility  bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \
taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \nmu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29 mumaxn.cvt=1417 \nmumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \ncsp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 betan.cvt=2 betap.cvt=2 \n pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14
4. Specified Contacts used & Interface fixed charge

# contact name=gate n.poly
#
interface s.n=0.0 s.p=0.0 qf=3e10
#

5. Numerical method used

# method newton gummel itlimit=25
trap atrap=0.5 maxtrap=4 autonr 
nrcriterion=0.1 tol.time=0.005
dt.min=1e-25 damped delta=0.5 
damploop=10 dfactor=10 iccg
lu1cri=0.003 lu2cri=0.03
maxinner=25
log outf=NMOS100a.log
6. To generate Drain current Vs Gate Voltage (Transfer characteristics)

#
solve init
solve vdrain=0.1
solve vgate=0 vstep=0.25 vfinal=3.0
   name=gate
#
tonyplot NMOS100a.log
#
7. Output Characteristics

#
solve vgate=1 outf=solve1
solve vgate=2 outf=solve2
solve vgate=3 outf=solve3
#
load infile=solve1
log outfile=NMOS2-1a.log
solve name=drain vdrain=0 vfinal=3 vstep=0.2
#
load infile=solve2
log outfile=NMOS2-2a.log
solve name=drain vdrain=0 vfinal=3 vstep=0.2
#
load infile=solve3
log outfile=NMOS2-3a.log
solve name=drain vdrain=0 vfinal=3 vstep=0.2
#
tonypplot -overlay NMOS2-1a.log NMOS2-2a.log NMOS2-3a.log
quit