CHAPTER 5:
Layout Design Rules
Introduction

Any circuit physical mask layout must conform to a set of geometric constraints or rules called as ‘Layout Design rules’ before it can be manufactured using particular process.

The rules specify minimum allowable line widths for physical objects on-chip such as Metal & PolySi interconnects or diffusion areas, feature dimension and so on.

For example:
1. If metal line width is too small, it is possible for the line to break during fabrication process and result of open circuits
2. If the lines are places too closed to each other, it may form an unwanted short circuit by merging during or after fabrication process

Main objective of ‘Layout design Rules’ is to achieve, for any circuit to be manufactured with a particular process, a high overall yield and reliability while using the smallest possible silicon area.
Simple NMOS Transistor Layout

- **S** (Source) connected to **n** (Substrate) and **p** (P-Substrate)
- **D** (Drain) connected to **n** (Substrate) and **p** (P-Substrate)
- **G** (Gate) connected above the **n** (Substrate) and **p** (P-Substrate)

**Silicon Oxide Insulator**

**Field Induced N-channel**

**Thin Oxide**

**PolySi**

**Gate Length**

**Active Area Mask**
Simple NMOS Transistor Layout

- Active area mask defines the extent of Thick Oxide.
- Polysilicon mask also controls the extent of Thin Oxide (@ Gate Oxide).
- N-type implant has no extra mask:
  - It is blocked by thick oxide & polysilicon.
  - The implants is self-aligned.
- Substrate connection is to the bottom of wafer.
  - All substrates is to ground.
NMOS Transistor

Where it is not suitable for substrate connections to be shared, a more complex process is used.

- Five Masks must be used to define the transistor:
  1. P well - For Isolation
  2. Active Area
  3. PolySilicon
  4. N+ Implant
  5. P+ Implant
CMOS Inverter

Input → Vdd → Output

Gnd

N well
P implant
N implant
Active Area
PolySi
Contact Window
Metal

Vdd
IN
OUT
GND

TAPS

TAPS – Substrate Connection
The process described here is an N well process since it has only an N well. P well & Twin Tub processes also exist. Note that the P-N junction between chip substrate and N well will remain reverse biased / 0 V. Thus, the transistors remain isolated. N implant defines NMOS source/drain and PMOS substrate contact. P implant defines PMOS source/drain and NMOS substrate contact.

CMOS Inverter
Stick Diagram

- Explore your design space since it can give:
  - Implications of crossovers
  - Numbers of contacts
  - Arrangement of devices & connections

- Process Independent layout but Technology dependent

- Easy to expand to a full layout for a particular process:
  - Magic (symbolic editor)
  - Tanner tools
Stick Diagram of CMOS Inverter

Vdd

IN

OUT

GND

TAPS

TAPS

Metal (Blue)

Contact

Polyisilicon (Red)

Combined

contact + Taps

N+ (Green)

P+ (Yellow)
Note that different style of layout will affect the overall performance of the device such as silicon area, timing, parasitic effect and so on

Thus, careful selection of layout style is crucial and must be carefully taken care

Exercise: Draw the stick diagram of AND, OR, NOR, EX-OR
For complex Logic gates, all complementary gates may be designed using a single row of n-transistors above or below a single row of p-transistors, aligned at common gate connections.

Thus, in this layout style:

1. The gates are designed using unbroken row of transistors in which abutting source-drain connections are made.

2. This called as “line of diffusion” rule, since the transistors form a line of diffusion intersected by polysilicon gate connections.
Complex Logic Gates Layout

- However in this layout style, the gate arrangement must be find first by:
  1. Careful selection of transistor ordering
  2. Careful orientation of transistor source and drain
- Method use for finding optimum gate ordering/orientation called as "Euler Path" where all complex circuits is:
  1. First converted to Euler path of p-network and n-network graph
  2. Then find the common Euler path for both graph
- The Euler path is defined as an uninterrupted path that transverse each edge (branch) of the graph exactly once only.
- Example:
  1. Draw the CMOS logic gate of the Boolean function of:

\[ Z = \frac{A(D + E)}{BC} \]
Complex Logic Gates Layout

\[ Z = A(D + E) + BC \]
Finding An Euler Path

- Exercise: Sketch the CMOS logic circuits, CMOS logic symbol, find the Euler Path & Sketch the Stick Diagram of the following Boolean Function:

1. \( Z = (AC) + B \)
2. \( Z = (A + B + C)(D + E)F \)
3. \( F = ((AB) + (CD)) \)
4. \( F = ((A + B + C)D \)
5. \( F = (A + B)C \)
6. \( F = (ABC) + (DE) + F \)
Finding An Euler Path

\[ Z = (AC) + B \]

\[ \text{Z} \]

- **Logic Circuits**
- **Logic Symbol**
- **p & n network graph**
- **Stick Diagram**

**The common Euler Path is C-A-B**

Note that the circuit has many common EP since it is a simple cct
Multiple Gates

Objective is to understand the method of making a layout of a system that consist of multiple gates.

Example:

- Gates can be abutted to create more complex functions.
- Gates should all be of same height
  - Power & Ground rails will then line up
- The output of one gate can be routed directly to the input of the next
- Note that this view is somewhat very simplistic but as inter-gate connections are usually more complex.
Multiple Gates

- All gate inputs and outputs are available at the top and bottom of the cells in polysilicon:
  - Routing of circuits is much easier
  - All routing is external to cells.
    - Thus, we can change inside of the cells without destroying circuit

Exercise: Make the layout of the multiple gates below

![Multiple Gates Diagram]

Multiplexer
Multi-cell Layout

- Objective is to explain a logical approach of implementing multi-cell layout
- All multi-cell layout consists of two stages:
  - Placement
  - Routing
- We have designed our cells with a constant height and with inputs and outputs at the top and bottom of the cell. Thus, we have the beginnings of a logical approach to multi-cell layout
- Placement: Cells are placed in one or several equal length with inter-digitized power and ground rails
Multi-cell Layout

- Two conductor routing: In the channels between the cells, we route metal horizontally and polysilicon vertically.
- This logical approach means that we should never have to worry about signals crossing.
- This make life considerably easier for a computer (or even a human) to complete the routing.
- We must only ensure that the two signals will not meet in the same horizontal or vertical channel.
- For most VLSI applications we have two layer metal processes.
- The norm is to use only metal for inter-cell routing and either Metal1 horizontally (for power rails) and metal2 vertically (for inputs and outputs) or vice versa.
LAYOUT USING TANNER

- Objective : To introduce the method of using CAD tools for making gates Layout i.e Tanner (L-edit, S-edit & T-Edit)
- S-Edit : is a powerful Schematic entry package, which can generate netlist directly usable in T-Spice simulations
- T-Edit : performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator can analyze large, complex designs with hundreds of thousands of circuit elements.
- L-Edit: layout tool that represents the masks that are used to fabricate an integrated circuit. In L-Edit, layers are associated with masks used in the fabrication process. Different layers can be conveniently represented by different colors and patterns.
CMOS Inverter

Step 1: Draw NMOS side first

- Rule 2.1: min 3 \( \lambda \)
- Rule 3.1: min 2 \( \lambda \)
- Rule 3.3: min 2 \( \lambda \)
- Rule 3.4: min 3 \( \lambda \)
- \( W_n = 5\lambda = 5\mu \)

Step 2: Source & Drain Contact

- Rule 6.1: 2 \( \lambda \)
- Rule 6.4: 2 \( \lambda \)
- Rule 7.3: 1 \( \lambda \)

Step 3: N-select Layer

Step 4: Connect to GND

Connect metal 1 at the bottom of NMOS and then connect them using active layer that overlaps with a metal 1.
Step 5: Using Via to Connect to GND

Rule 6.2: 1.5 \lambda
Rule 6.1: 2 \lambda

Rule 6.1: 2 \lambda.

Rule 3.5: 1 \lambda

Step 6: Taps/Bulk contact

Rule 4.2: 2 \lambda

Rule 4.3: 1 \lambda

Cover the bulk with a p-select layer. Note that the p-select and n-select layer may be coincident but cannot overlap.

Step 7: pmos side

Looks the same as the NMOS except that it is covered by a p-select layer.
Step 8: n-well for pmos

Step 9: Connect both nmos & pmos

Also connect the PMOS to Vdd. It’s the same as the NMOS connected to the Gnd.

Step 10: Final Layout

Used another poly to connect the Vdd and Gnd and connect it to the output so that we can connect this inverter to other cells in the future. At the intersection of metal 1 and poly, use a poly contact. Label appropriately.
\[ F = \left( \frac{A + B + C}{D} \right) \]

\[ Z = \left( \frac{A + B}{C} \right) \]

Diagram of electrical circuit with nodes A, B, C, D, Vdd, and GND.
\[ Z = (ABC) + (DE) + F \]
\[ F = (A \cdot S) + (B \cdot \overline{S}) \]